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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,470	11/20/2001	Akihiro Kirisawa	03830045AA	8763

7590 10/07/2005  
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EXAMINER

KENDALL, CHUCK O

ART UNIT	PAPER NUMBER
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2192

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/988,470

**Applicant(s)**

KIRISAWA, AKIHIRO

**Examiner**

Chuck O. Kendall

**Art Unit**

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This action is in response to the application filed 07/06/05.
2. Claims 1 – 15 are pending.

### Claim Rejections - 35 USC 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 –15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warmink USPN 6,301,709 B1 (art of record) in view of Bishop USPN 4,823,256 (art being made of record).

Regarding claim 1, Warmink anticipates a program updating system having a communication function comprising:

a first processor which operates by referring to a program stored therein (FIG. 1, see FIRST CIRCUIT PACT, 20 and associated text); and

a second processor which executes update of said program by using said communication function with an external unit, and executes an update control of said (FIG. 1, see SECOND CIRCUIT PACT, 30, and associated text for updating see, 4:12 – 17). Although, Warmink doesn't disclose the second processor executing the update control of said program when a fault of said first processor is detected, he does mention any circuit pack in memory may need to be upgraded at some point to fix bugs (errors in code). However, Bishop in an analogous art and similar configuration does disclose having and a first and second memory for a first and second processor which is automatically updated during fault recovery (16:45 – 17:10). Therefore it would have

been obvious to one of ordinary skill in the art at the time the invention was made to combine Warmink and Bishop, because it would have enabled the automatic recovery of code during fault detection.

Regarding claim 2, the program updating system having the communication function according to claim 1, wherein said second processor transmits a reset signal to said first processor for every predetermined cycles, and monitors a response pulse which is transmitted from said first processor in response to said reset signal, and transmits a compulsory reset signal to said first processor when said response pulse can not be detected within a predetermined period (Warmink, 2:32 - 55, see reset, also see Bishop 18:60 – 65).

Regarding claim 3, the program updating system having the communication function according to claim 2, further comprising;

an activation pulse generating circuit which generates an activation pulse to activate said second processor (4:20 – 25), wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse generating circuit (Warmink, 2:35 – 45, see receiving request and answering them, also see Bishop FIG. 12. 1003, and all associated text for freeze state of active processor).

Regarding claim 4, the program updating system having the communication function according to claim 3, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program in said buffer is completed (Warmink, 1 : 53 - 57, see memory storage area).

Regarding claim 5, the program updating system having the communication function according to claim 1, further comprising..

an activation pulse generating circuit which generates an activation pulse to activate said second processor, wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse

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generating circuit (Warmink, 2: 33 -35, for activation pulse see receiving reset and start).

Regarding claim 6, the program updating system having the communication function according to claim 5, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (Warmink, 1:55 - 65).

Regarding claim 7, the program updating system having the communication function according to claim 1, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (Warmink, 1 :55 - 65).

Regarding claim 8, the program updating system having the communication function according to claim 2, further comprising;

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse which is outputted from said second processor in response to said activation pulse, wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period (Warmink, 3:30 - 55, see reset and see answering request, also see 2:30 - 37, and 65 - 67, for circuit pack which did not receive signal (for pulse not detected)).

Regarding claim 9, the program updating system having the communication function according to claim 8, further comprising;

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (Warmink, 1:55 - 65).

Regarding claim 10, the program updating system having the communication function according to claim 1, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse outputted from said second processor in response to said activation pulse, wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period (Warmink, 3:30 - 55, see reset and see answering request, also see 2:30 - 39 and 65 - 67, for circuit pack which did not receive signal (for pulse not detected)).

Regarding claim 11, the program updating system having the communication function according to claim 10, further comprising;

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (Warmink, 1: 45 - 65).

Regarding claim 12, which recites the method version of claim 1, see rationale as previously discussed above.

Regarding claim 13, Warmink discloses all the claimed limitations as applied in claim 12 above. Warmink doesn't explicitly disclose wherein said second processor transfers said program obtained by using said communication function to said first processor, during a stop of said first processor, although Warmink does mention transmitting resetting signals (Warmink, 2:33 - 45). Bishop discloses in an analogous art stopping execution of normal tasks, to freeze the state of the active processor and reset the internal processor state to the second processor (21:50 - 65).

Therefore it would have been obvious to one of ordinary skills in the art at the time invention was made to combine Warmink and Bishop because stopping the processor would enable it to check its internal state before transferring control over to the second processor.

Regarding claim 14, Bishop further discloses the program updating method using the communication function according to claim 13, further comprising;

providing an activation control circuit which controls activation and a stop of said second processor, wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period (Bishop, see 13:45 – 50, for sanity timers).

Regarding claim 15, the program updating method using the communication function according to claim 12, further comprising; providing an activation control circuit which controls activation and a stop of said second processor, wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period (Warmink, 3:30 - 55, see reset and see answering request, also see 2:30 - 37, and 65 - 67, for circuit pack which did not receive signal (for pulse not detected)).

### ***Response to Arguments***

5. Examiner is withdrawing the previous Final rejection of 05/25/05. However, Applicant's arguments with respect to claims 1 - 15 have been considered but are moot in view of the new ground(s) of rejection.

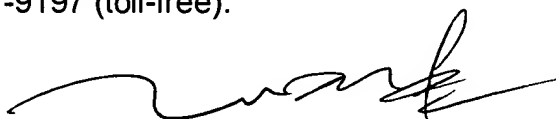
### Correspondence information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.



TUAN DAM  
SUPERVISORY PATENT EXAMINER